REMARKS

The three-month period for responding to the last Office Action ended on December 29, 2003. A request for a two-month extension of time and the associated fee is enclosed. Accordingly, this Amendment is timely filed.

By this Amendment, claims 1 and 28 are being amended, and new claim 31 added to more particularly point out and distinctly claim the subject invention. Claims 1-31 remain in this case.

Claim 1 stands rejected under 35 U.S.C. 102(b) as allegedly anticipated by Sakurai et al. (EP 0 032 022), and claims 2-30 stand rejected under 35 U.S.C. 103(a) as allegedly obvious over the same reference, further in view of the Examiner's comments regarding routine experimentation or Nemoto (JP 9027551). These rejections, to the extent that they are deemed applicable to the claims as now presented, are respectfully, but most strenuously traversed.

Claim 1 has been amended to specify that the "production of additional n-doped and/or p-doped areas in the p-doped or n-doped inner area and in the fringe area of the n-doped or p-doped trough that form the structure of the semiconductor component" does not involve "a step of additional doping of the p-doped inner area or n-doped inner area to prevent turnover of conductivity type."

This process is not taught by the applied prior art and, is, in fact, contrary to the teaching of the primary reference.

It has already been established in the prosecution history of this application, that:

1. In the invention of Sakurai et al., as illustrated in Figures 7-11 of that reference, an inner active region 101A of the silicon substrate 101, surrounded by the N^+ type buried layer 105, is inverted to an N^- type region, and an additional implantation step is necessary to form a P type base region 107 on the active region 101A. See pages 5 and 6 of the amendment dated December 12, 2002.
2. Figures 2-6, described in the background section of the Sakurai et al. reference discloses a N^+ type buried layer formed by phosphorous ions implantation in a P type silicon semiconductor substrate 21. The general description of this earlier method in the Sakurai et al. reference does not specify the implantation energy used to create the N^+ type buried layer 24 in the P type semiconductor substrate 21, but does describe the region 26 surrounded by the N^+ type buried layer 24 as P type. Thus, the Examiner has inferred from this general description of the earlier

method that an implantation energy is employed that leaves a trough enclosed surface area with the same doping as the original substrate.

3. At page 2, lines 20-25, Sakurai states that the described earlier method was proposed in Japanese patent application No. 50-364. A copy of this Japanese patent application and an English translation thereof were provided with Applicants' Request for Reconsideration dated August 5, 2003.

4. The Japanese reference (Inayoshi) discloses a method for producing semiconductor components, wherein an implant energy of 1 MeV is used. Figure 3 of this reference suggests that the inner area 4, above the trough 3, retains the same donor type as the original substrate after implantation. Inayoshi teaches a further step "For improving the performance, in particular, namely for preventing turnover of conductivity type in board 1, boron ion is injected into board 1 with low concentration, and P^+ type layer 5 is formed." (See paragraph (5) of translation and Figure 4 of Japanese reference.) Thereafter, an additional N^+ doped area 7 is formed in inner area 4.

In contrast to the teachings of Inayoshi and Sakurai, the present invention does not employ a step of additional doping of the p-doped inner area or n-doped inner area to prevent turnover of conductivity type. Claim 1 has been amended to explicitly recite this distinction.

An important aspect of the present invention is the use of a high implantation energy with respect to the implantation dose, so that the doping of the region surrounded by the buried layer does not change, i.e. the region surrounded by the buried layer has the same doping as the starting semiconductor substrate. Therefore, the method according to the invention does not require an additional compensation step to revert the inner surface area to the doping of the original substrate. Further the production of additional n-doped and/or p-doped areas in the p-doped or n-doped inner area does not require additional doping to prevent turnover of conductivity in order to create a semiconductor structure for producing a semiconductor component.

Enclosed herewith is an article entitled ANALYTICAL DESCRIPTION OF HIGH ENERGY IMPLANTATION PROFILES by L. GONG et al as evidence that Fig. 3 of Inayoshi is wrong. The experimental profiles of Fig. 9, page 393 confirm the analytical description of Fig. 2 of the amendment dated December 12, 2002.

It is noted that a starting substrate having a doping of very low concentration is usually used. It is an important advantage of the method according to the invention that the region surrounded by the buried layer is the remaining virgin material of the substrate without any change of doping level to a well defined depth. High energy ions implanted for generating the buried layer pass through this zone with very little impact on the crystal, i.e., they interfere mainly with the electrons. Such damage can be easily annealed. This is in sharp contrast to a compensation method, where the ions of the implanted buried layer and the compensating ions are interfering both with the nucleus of the crystal. Depending on dose and energy of the ions, the crystal damage cannot be annealed completely and may have a very negative influence on the quality of the pn-junctions in this part of the devices. Crystal damage is a drawback of high energy implantation and becomes even more severe by compensation.

To produce bipolar semiconductor elements with reasonable breakdown voltage one needs damage free semiconductor material of a certain depth. The doping concentration should be some 10^{15} ions/cm^3 or less. Measurements of L. Gong et al demonstrate that phosphorous implants with an energy of 1.3 McV and a dose of 10^{15} ions/cm^2 have a concentration of more than 10^{17} ions/cm^3 at the surface. In a depth of 1 mm it is 1.5 order of magnitude higher. It is obvious that two or three orders of magnitude are impossible to anneal by implantation if one needs a resulting accuracy of approximately 10% of a doping concentration of some 10^{15} ions/cm^3. One limiting factor is the accuracy of ion implanters. The other reason is that no twist and tilt angles exist to avoid channeling on all areas of a wafer. Channeling reduces the ion-concentration to a large extent at high ion energy. The compensating phosphorous and boron ions have different atomic weight and therefore different channeling properties. This reduces the accuracy additionally. The doping of very low concentration of the region surrounded by the buried layer is a feature which distinguishes the semiconductor substrate as produced with the method steps according to the invention, from the structure as disclosed in EP 0 232 022 (Sakurai) and JP NO. 50.364 (Inayoshi).

EP 0 232 022 and JP NO. 50.364 uses a high dose for the additional implantation so that the doping of the inner region has a high concentration (p^+) with respect to the very low concentration (p^-) of the substrate's doping. This highly doped layer is used for the base of an npn transistor.

The prior art is devoid of any teaching or suggestion to produce semiconductor components by using the semiconductor structure as produced with the method steps of claim 1 without the step of an additional compensation step to prevent turnover of conductivity type.

There was a widely held but incorrect opinion of the experts of the technical field that a semiconductor structure as produced by the method steps of claim 1 which is characterized by the same (very low) concentration of the doping of the substrate and the inner region cannot be used for producing semiconductor components, e.g. an I^2L-element.

The prior art is devoid of any teaching or suggestion to use the above structure for creating semiconductor elements using the semiconductor structure as produced with the method steps according to the invention. The inventor has proposed to create semiconductor components having improved properties using the semiconductor structure in question, e.g. an I^2L-element. With respect to these advantages, reference is made to pages 4 and 5 of the last Amendment.

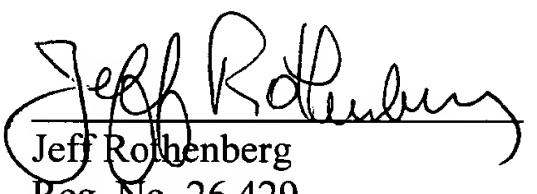
Applicant submits that it is not obvious for the skilled person to use the semiconductor structure in question for producing semiconductor components.

For all of the above reasons, independent claim 1 is believed to be allowable. The dependent claims are allowable for the same reasons as independent claim 1 from which they all ultimately depend as well as for their additional limitations.

Favorable reconsideration and allowance of this application is respectfully requested.

If it would advance the prosecution of this application, the Examiner is invited to contact Applicants' representative at the below listed telephone number.

Respectfully submitted,



Jeff Rothenberg
Reg. No. 26,429
Attorney for Applicant

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Heslin Rothenberg Farley & Mesiti P.C.
5 Columbia Circle
Albany, New York 12203
Tel: 518-452-5600
Fax: 518-452-5579
E-mail: jr@hrfmlaw.com